3. (Once amended) The sense amplifier of claim 1, wherein the drain region for the [pair of transistors] dual-gate transistor and the drain region for the transistor of the first conductivity type in one inverter is further coupled to a gate of the transistor of a first conductivity type and to a second gate of [a second one of the pair of transistors] the dual-gate transistor in the other inverter.

4. (Once amended) A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a [pair of] dual-gate n-channel metal oxide semiconductor (NMOS) [transistors] transistor [coupled at a drain region and a source region, and] wherein a drain region of the PMOS transistor is coupled to [the] a drain region for the [pair of NMOS transistors] dual-gate NMOS transistor;

a bit line coupled to each inverter, wherein each bit line couples to a first gate [for a first one] of the [pair of NMOS transistors] dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region for the PMOS and the [NMOS transistors] dual-gate NMOS transistors.

5. (Once amended) The sense amplifier of claim 4, wherein the drain region for the PMOS and the dual-gate NMOS transistors in one of the cross-coupled inverters is further coupled to a gate of the PMOS transistor and to a second gate of [a second one of the pair of NMOS transistors] the dual-gate NMOS transistor in the other one of the cross-coupled inverters.

10. (Once amended) A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a [second transistor and a third transistor] dual-gate transistor of a second conductivity type, [wherein the second and third transistors are coupled at a drain region and are coupled at a source region, and] wherein [the] a drain region for the [second and

third transistors] dual-gate transistor [are] is coupled to a drain region of the first transistor;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a first gate of the [second transistor] dual-gate transistor in each amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the [second and the third transistors] dual-gate transistor.

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11. (Once amended) The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the [second and the third transistors include] dual-gate transistor includes an n-channel metal oxide semiconductor (NMOS) [transistors] transistor.

12. (Once amended) The latch circuit of claim 11, wherein the drain region for the PMOS and the [NMOS transistors] dual-gate NMOS transistor in one of the cross-coupled amplifiers is further coupled to a gate of the PMOS transistor and to a second gate of [a third transistor] the dual-gate NMOS transistor in the other one of the cross-coupled amplifiers.

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18. (Once amended) The amplifier circuit of claim 17, wherein the transistor of a first conductivity type includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the [a] dual-gated MOSFET of a second conductivity type is divided into two separate n-channel metal oxide semiconductor (NMOS) transistors each driven by one of the dual gates.

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23. (Once amended) A memory circuit, comprising:

a number of memory arrays;

at lease one sense amplifier, wherein the sense amplifier includes:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a [pair of n-channel] dual-gate metal oxide semiconductor (NMOS) [transistors] transistor [coupled at a drain region and a source region, and]

wherein a drain region of the PMOS transistor is coupled to [the] a drain region for the [pair of NMOS transistors] dual-gate NMOS transistor;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in the number of memory arrays, and wherein each one of the complementary pair of bit lines couples to a first gate of [a first one of the pair of NMOS transistors] the dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the [pair of NMOS transistors] dual-gate NMOS transistor in each inverter.

25. (Once amended) The memory circuit of claim 23, wherein the drain region for the PMOS and the dual-gate NMOS transistors in one of the cross-coupled inverters is further coupled to a gate of the PMOS transistor and to a second gate of [a second one of the pair of NMOS transistors] the dual-gate NMOS transistor in the other one of the cross-coupled inverters.

29. (Once amended) An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a [pair of n-channel] dual-gate metal oxide semiconductor (NMOS) [transistors] transistor [coupled at a drain region and a source region, and] wherein a drain region of the PMOS transistor is coupled to [the] a drain region for the [pair of NMOS transistors] dual-gate NMOS transistor;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the

complementary pair of bit lines couples to a first gate of [a first one of the pair of NMOS transistors] the dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the [pair of NMOS transistors] dual-gate NMOS transistor in each inverter.

32. (Once amended) An integrated circuit, comprising:

a processor;

a memory operatively coupled to the processor; and

wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a [pair of transistors] dual-gate transistor of a second conductivity type [coupled at a drain region and coupled at a source region, and]

wherein [the] a drain region for the [pair of transistors] dual-gate transistor is coupled to a drain region of the transistor of the first conductivity type;

a pair of bit lines, wherein each one of the pair of bit lines is coupled to a first gate of [a first one of the pair of transistors] the dual-gate transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the [pair of transistors] dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter.

33. (Once amended) A method for forming a current sense amplifier, comprising:

cross coupling a pair of inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a [pair of transistors] dual-gate transistor of a second conductivity type [coupled at a drain region and coupled at a source region, and] wherein [the] a drain region for the

[pair of transistors] dual-gate transistor is coupled to a drain region of the transistor of the first conductivity type; and

wherein cross coupling the pair of inverters includes coupling the drain region for the transistor of the first conductivity type and the drain region for the [pair of transistors] dual-gate transistor in one inverter to a gate of the transistor of a first conductivity type and to a second gate of [a first one of the pair of transistors] the dual-gate transistor in the other inverter.

34. (Once amended) The method of claim 33, wherein cross coupling the pair of inverters includes forming the first transistor of the first conductivity type as a p-channel metal oxide semiconductor (PMOS) transistor, and forming the [pair of transistors] dual-gate transistor of a second conductivity type as an n-channel metal oxide semiconductor (NMOS) [transistors] transistor.

35. (Once amended) The method of claim 33, wherein the method further includes coupling a bit line to a first gate of [a second one of the pair of transistors] the dual-gate transistor in each inverter.

36. (Once amended) The method of claim 33, wherein the method further includes coupling an output transmission line to the drain region for the [pair of transistors] dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter.

37. (Once amended) A method for forming a sense amplifier, comprising:

forming and cross coupling a pair of inverters, wherein forming and cross coupling each inverter includes:

forming a first transistor of a first conductivity type;

forming a [second transistor and a third transistor] dual-gate transistor of a second conductivity type, wherein forming the [second and the third transistors] dual-gate transistor includes [coupling a drain region and a source region for the second and third transistors, and] coupling the drain region for the [second and third transistors] dual-gate transistor to a drain region of the first transistor;

coupling a bit line to a first gate of the [second transistor] dual-gate transistor in each inverter; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the [second and the third transistors] dual-gate transistor in each inverter.

38. (Once amended) The method of claim 37, wherein forming the first transistor of a first conductivity type includes forming a p-channel metal oxide semiconductor (PMOS) transistor, and wherein forming the [second and third transistors] dual-gate transistor of a second conductivity type includes forming an n-channel metal oxide semiconductor (NMOS) [transistors] transistor.

39. (Once amended) The method of claim 37, wherein cross coupling the pair of inverters includes coupling the drain region for [second and third transistors] the dual-gate transistor and the drain region for the first transistor of the first conductivity type in one inverter to a gate of the first transistor of a first conductivity type and to a second gate of [a third transistor] the dual-gate transistor in the other inverter.

40. (Once amended) A method for operating a sense amplifier, comprising:

equilibrating a first and second bit line, wherein the first bit line is coupled to a first gate of a [first NMOS transistor] dual-gate transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a first gate of a [first NMOS transistor] dual-gate transistor in a second inverter in the sense amplifier;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter to a gate of a PMOS transistor and to a second gate of a [second NMOS transistor] dual-gate transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a second gate of a [second NMOS transistor] dual-gate transistor in the first inverter.

44. (Once amended) A method for operating a sense amplifier, comprising:

providing a first bit line signal to a first gate of a [first NMOS transistor] dual-gate transistor [coupled at a drain region and a source region to a second NMOS transistor] in a first inverter of the sense amplifier;

providing a second bit line signal to a first gate of a [first NMOS transistor] dual-gate transistor [coupled at a drain region and a source region to a second NMOS transistor] in a second inverter of the sense amplifier; and

wherein providing the first and the second bit line signals to the first gates of the [first and second NMOS transistors] dual-gate transistors isolates the bit line capacitances from a first and second output node on the sense amplifier.

45. (Once amended) A method for operating a sense amplifier, comprising:

providing an input signal from a bit line to a first gate of a [first transistor] dual-gate transistor in a first inverter of the sense amplifier; and

wherein providing the input signal to the first gate of the [first transistor] dual-gate transistor isolates the bit line capacitance from an output node on the sense amplifier.

REMARKS

Claims 1-5, 10-12, 18, 23, 25, 29, 32-40, 44, and 45 are amended, no claims are canceled, and no claims are added; as a result, claims 1-45 are pending in this application.

Rejection under 35 U.S.C. §102(b)

Claims 1-16, 29-39, 44, and 45 were rejected under 35 U.S.C. §102(b) as being anticipated by Kawashima (US Patent No. 5699305). Examiner's rejection states:

> Kawashima describes in figure 7 a sense amplifier comprising: a pair of cross coupled inverters (66-69, and 72-75), wherein each inverter includes: a transistor of a first conductivity type (66, 67), a pair of transistors of a second conductivity type (68, 69, 74, 75) coupled at a drain region and coupled at a source region, and wherein the drain region for the pair of transistors is coupled to a drain region of the transistor of the first conductivity type; a pair of bit lines (IN, /IN), wherein each one of the pair of bit lines is coupled to a gate of a first one of the pair of transistors in each inverter; and a pair of output transmission lines (OUT, /OUT), wherein each one of the pair of output